ABSTRACT OF THE DISCLOSURE

In order to provide a comparator circuit without generating a malfunction, the comparator circuit according to the present invention may comprise a comparator circuit including a differential amplification circuit having a differential pair transistor (M1, M2) for inputting a signal as an object of comparison, and a current mirror load circuit (M3, M4, M5, M6); a latch circuit having inversion amplifiers that are configured so that an input of one amplifier becomes an input of other amplifier so as to amplify a differential output signal outputted from the current mirror load circuit in accordance with a magnitude relation of the signal as an object of comparison; an equalization transistor (M9) for equalizing a signal of the differential amplification circuit; a delay circuit (M13, M14,M15, M16) for generating a signal to delay a control signal to be inputted in a control electrode of the equalization transistor; and a control transistor (M10) for inputting an output signal of the delay circuit in the control electrode as a control signal to make the latch circuit into an active status and a non-active status.